

## Description

The ISL54059EVAL1Z, ISL54060EVAL1Z, ISL54061EVAL1Z, ISL54062EVAL1Z, ISL54063EVAL1Z and ISL54064EVAL1Z evaluation board is designed to provide a quick and easy method for evaluating the ISL54059 through ISL54064 ICs.

The ISL54059 and ISL54062 ICs are a single supply Dual Single-Pole Double Throw (SPDT) analog switches while the ISL54060, ISL54061, ISL54063 and ISL54064 IC's are single supply Dual Single-Pole Single Throw (SPST) analog switches. All devices feature negative swing capability, sub- $\Omega$  ON-resistance, and low power dissipation. The ICs are designed for applications that require an analog switch that may see voltages below ground at the switch terminals, such as audio and video. The evaluation board is developed to evaluate the ISL540XX ICs, integrating many features for ease of use in examining the performance of the device under various operating conditions. To help understand the operation of the ISL540XX IC and the ISL540XXEVAL1Z evaluation board, it is recommended to study the evaluation board schematic found on page 4 of this document and the datasheet for the IC under evaluation.

The ICs are analog switches that are capable of swinging down to 6.5V below the positive supply rail. For example, if the supply is at +1.8V, the switch terminal analog operating range is from -4.3V to +1.8V. The ISL54062, ISL54063, and ISL54064 also integrate Click and Pop Elimination Circuitry to remove transient noises at the speaker during power ON/OFF of an audio system. The evaluation board contains standard RCA/BNC connectors and a single headphone jack to allow the user to easily interface with the IC to evaluate its functions, features, and performance.

This application note will guide the user through the process of configuring and using the evaluation board to evaluate the ISL540XX devices.

## Key Features

- RCA Audio Input/Output Jacks, Stereo Headphone Output Jack and BNC Connectors
- Convenient Test Points and Connections for Test Equipment
- Click and Pop Elimination Circuitry (ISL54062, ISL54063, and ISL54064)
- Manual or External Logic Input Control

## Picture of Evaluation Board (Top View)



FIGURE 1. ISL54059EVAL1Z THROUGH ISL54064EVAL1Z EVALUATION BOARD

## Board Architecture/Layout

### Basic Layout of Evaluation Board

A picture of the evaluation board is located in Figure 1. The ISL540XX IC is located inside socket U1 located at the center of the evaluation board. The IC needs to be orientated inside the socket such that the pin 1 indicator on the IC is aligned with the pin 1 indicator dot inside the socket. The evaluation board integrates the necessary connections and components to interface with the ICs for ease of operation.

### Power Supply

The ISL540XX IC requires a supply voltage in the range of +1.8V to +6.5V for proper operation. Banana jacks for  $V_{CC}$  (J1) and GND (J2) are located at the top of the board. The evaluation board contains a 10 $\mu$ F bulk capacitor and a 0.1 $\mu$ F high frequency decoupling capacitor at the supply lines.

### Logic Control

The evaluation board contains two types of logic control to the digital logic inputs of the IC available to the user. The logic pins can be controlled either through manual or external operation. The logic control pins are manually toggled by the SPST switches mounted on the evaluation board (S1-S2). When the switch is in the up position (H), the associated logic pin is pulled to  $V_{CC}$  for logic HIGH. When the switch is in the down position (L), the associated logic pin is pulled to GND for logic LOW. For manual operation, the jumpers JP6-JP7 need to be in the 2-3 position.

For external control via a function generator or switched source, set the jumpers JP6-JP7 in the 1-2 position. This by-passes the SPST switches and routes the logic control to

the BNC connectors J13-J14 located on the bottom right side of the board.

Note: There are 500kΩ logic pull-down resistors on the INx control pins. In external control mode when the digital logic input lines are left in a floating state, these pull-down resistors bias the logic inputs to ground.

### Switch Terminals

The evaluation board contains components to interface with all six terminals of the Dual SPDT switch (four terminals for the SPST switches). The common (COM) terminals of the switch are located on the right side of the evaluation board. The Normally Open (NO) and Normally Closed (NC) terminals of the switch are located on the left side of the evaluation board. All switch terminals include both RCA jacks and BNC connectors. The COM terminals also include a headphone jack (HJ1) for connecting a stereo headphone or line level plug.

Note: There are 10kΩ pull-down resistors on the NCx and NOx pins of the evaluation board (R21, R22, R23, and R26). They will need to be depopulated if the user does not desire to have them.

Refer to Table 1 for a list of the connections on the ISL540XXEVAL1Z and the associated pin of the IC. The evaluation board also includes Test Points for convenient locations to probe specific pins on the IC.

**TABLE 1. BOARD COMPONENT TABLE**

DEVICE PIN	EVALUATION BOARD CONNECTION	TEST POINT	APPLICABLE IC
V <sub>CC</sub>	J1	TP1	All
GND	J2	TP2	All
IN1	S2, J13	TP8	All
IN2	S1, J14	TP9	All
NO1	J11, J12	TP7	ISL54059, ISL54060, ISL54062, ISL54063
NC1	J5, J6	TP4	ISL54059, ISL54061, ISL54062, ISL54064
COM1	J3, J4, HJ1	TP3	All
NO2	J15, J16	TP10	ISL54059, ISL54060, ISL54062, ISL54063
NC2	J7, J8	TP5	ISL54059, ISL54061, ISL54062, ISL54064
COM2	J9, J10, HJ1	TP6	All

Note: All switch terminals on the evaluation board have place holders that can have surface mounted components placed either in series with the switch path or shunted to ground. Jumpers on these components allow flexible configurations. Refer to the Evaluation Board Schematics located on page 4 for clarification.

### Power Supply

The DC power supply connected at banana jacks J1 (V<sub>CC</sub>) and J2 (GND) provides power to the evaluation board. The evaluation board requires a +1.8V to +6.5V DC power supply for proper operation. The power supply should be capable of delivering 100μA of current.

### Logic Control

The state of the ISL540XX IC is determined by the Truth Table as defined in their respective datasheet. When in manual operation mode, the logic being toggled by the SPST switches (S1-S2) will always drive the voltage of the logic pin to V<sub>CC</sub> for a HIGH and GND for a LOW. In external control mode, the voltages being driven by an external source must meet appropriate V<sub>IH</sub> and V<sub>IL</sub> levels as defined in the datasheet.

The control pins are 1.8V logic compatible up to a +3.3V supply, which allows for control via a standard μcontroller.  
Logic "0" (LOW) when ≤ 0.5V (or floating)  
Logic "1" (HIGH) when ≥ 1.4V

When operating above +3.3V supply, refer to the datasheet for appropriate logic levels to drive the logic pins. It is always recommended to drive the logic pins to the positive supply rail (V<sub>CC</sub>) and GND to minimize power consumption.

### Logic States

#### INPUT SELECT (INX) PINS

If the INx Pins are logic "HIGH", then the NOx switches are turned ON and the NCx switches are turned OFF. If the INx Pins are logic "LOW", then the NCx switches are turned ON and the NCx switches are turned OFF.

#### CLICK AND POP OPERATION (ISL54062, ISL54063, ISL54064 ONLY)

Single supply audio sources are biased at a DC offset that generates transients during power ON/OFF of the audio source. This DC offset is coupled through a blocking capacitor that is need to remove the DC bias to the speaker, causing a transient voltage at the load. For example, when the source is OFF and suddenly turned ON with a DC offset, the capacitor will develop a voltage equal to the DC offset. This voltage gets discharged by the speaker causing a click and pop noise. The ISL54062, ISL54063, and ISL54064 ICs integrate circuitry to eliminate click and pop noises to the speaker.

For proper operation of Click and Pop elimination, the switch terminal that is being connected to the speaker should be connected through the integrated shunt resistor before



# ISL54059EVAL1Z Through ISL54064EVAL1Z Evaluation Board Schematic

